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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 1400.4100242

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on 07-13-2009

Signature: /Ross D. Snyder/

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Application Number	Filed
09/495,207	01-31-2000

First Named Inventor: Robert E. Robotham

Art Unit	Examiner
2419	Weidner, Timothy J.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 37,730
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Robert E. Robotham

Title: METHOD AND APPARATUS FOR MERGING VIRTUAL CONNECTIONS

App. No.: 09/495,207 Filed: 01-31-2000

Examiner: Weidner, Timothy J. Group Art Unit: 2419

Atty. Dkt. No. 1400.4100242

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Claims 1-37 are pending in this application. The Examiner has rejected claims 1-37. Appellant respectfully requests reconsideration of pending claims 1-37. Appellant files herewith a notice of appeal. Pursuant to the "New Pre-Appeal Brief Conference Pilot Program," 1296 Off. Gaz. Pat. Office 67 (July 12, 2005) and the "Extension of the Pilot Pre-Appeal Brief Conference Program" dated 1/10/2006, Appellant submits a pre-appeal brief request for review. The review is requested for the reasons set forth below:

Appellant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection. Appellant submits the Examiner's "Response to Arguments" provides evidence that the Examiner has failed to consider the pending claims as required by the Manual of Patent Examining Procedure (MPEP) and prevailing case law. Applicant submits MPEP § 2141 sets forth the Graham inquiries for a rejection under 35 U.S.C. § 103. MPEP § 2143 describes examples of basic requirements of a *prima facie* case of obviousness under 35 U.S.C. § 103. As Appellant describes in detail below, Appellant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection.

The Examiner has rejected claims 1-37 under 35 U.S.C. §103(a) as allegedly being unpatentable over Sorinsuo et al. (U.S. Patent No. 6,148,001) in view of Shimojo (U.S. Patent No. 6,934,296)." Regarding claims 1, 10, 17, and 25, Applicant submits the mere teaching of "The state is maintained for each incoming VCC, which indicates whether the buffer of that VCC contains one or more complete AAL-5 packet" of col. 9, lines 14-16, of the Sorinsuo reference does not disclose or suggest "queuing the identity of a virtual connection...." Moreover, Applicant disagrees with the Examiner's assertion that "Shimojo, which is in the same field of

endeavor, teaches queuing a VCI for use in a buffer pointer management unit that associates the VCI with various connection parameters, and for outputting the data accordingly" is disclosed in "(columns 17 and 18, lines 19-31 and 49-57 respectively)" of the Shimojo reference. Moreover, Applicant submits even if such assertion were true, combining such assertion with the purported teachings of the Sorinsuo reference would not yield "queuing the identity of a virtual connection...."

As an example, Applicant submits the cited portions of the cited references do not disclose or suggest "queuing the identity of a virtual connection...." Applicant notes the Examiner does not allege the cited portions of the Shimojo reference as teaching, for example, "...when data that constitute a complete packet are buffered in a corresponding buffer." Rather, the Examiner alleges "It would have been obvious to one of ordinary skill in the art at the time the invention was made to queue the identity for when data that constitute a complete packet is [sic] buffered to associate the VCI with various connection parameters, and to output the data accordingly." However, Applicant notes MPEP § 2143 sets forth seven exemplary rationales that may support a conclusion of obviousness. Applicant submits the Examiner merely alleges "It would have been obvious to one of ordinary skill in the art...," but doesn't appear to apply any of the specific exemplary rationales recited in MPEP § 2143 or any other well-reasoned rationale consistent with relevant case law. Moreover, while the Examiner alleges, "Further, the combination yields predictable results," Applicant submits the Examiner does not provide any rationale for supposedly having reached that conclusion. In accordance with MPEP § 2143, Applicant submits the Examiner has not made a *prima facie* showing of unpatentability as to the subject matter of claims 1, 10, 17, and 25. Further, Applicant submits claims 1, 10, 17, and 25 do not claim "prioritization" as a mere "concept." Rather, Applicant submits "various priority options including the treatment of OAM cells" fails to disclose or suggest "obtaining prioritization information for the merged virtual connection." As another example, Applicant submits the Examiner does not show how the Examiner's allegation of "Sorinsuo further teaches various priority options including the treatment of OAM cells" supposedly justifies the conclusion "i.e., obtaining prioritization information." Applicant notes the portion of the Sorinsuo reference cited by the Examiner appears not to even mention "prioritization." Also, Applicant does not find any teaching of "X" disclosing a "merged identifier" either in Fig. 9 or in the description of Fig. 9 found in column 9 of the Sorinsuo reference. Thus, Applicant submits, even considering the cited portions in context and as a whole, Applicant submits the cited portions of the cited references fail to render the teaching asserted by the Examiner. As yet another example, while the Examiner cites "(figure 9, item 960, X)" as allegedly disclosing "the merged identifier," Applicant can see no teaching as to a mere representation of the letter "X" disclosing a "merged identifier." While Applicant provides examples from claim 1, Applicant notes the Examiner has not addressed claims 10 or 17 individually, so Applicant submits claims 10 and 17 are also not shown to be unpatentable.

Regarding claim 25, while the Examiner alleges "The Shimojo reference was used to show class-prioritized dequeuing in intervals (columns 24 and 25, lines 39-46 and 3-8)" and "They are in the same context

of class-prioritize buffers Ba1 and Ba2," Applicant submits those portions of the cited reference do not disclose all of the teachings alleged by the Examiner. As an example, Applicant doesn't see any teaching as to Ba1 in reference to "different ones of the intervals." As another example, Applicant sees no teaching as to "performed in intervals" or "for different ones of the intervals" in the cited portion. Applicant sees no teaching in "(column 24, lines 39-46)" as to "where different classes receive priority for different ones of the intervals" in the context of the supposed "intervals" of "(column 25, lines 3-8)."

Regarding claims 2, 18, and 26, Applicant submits claims 2, 18, and 26 do not claim "prioritization" as a "concept." Rather, Applicant notes the Examiner alleges "Packets are transmitted in the order that complete packets are received including when OAM cells are buffered as ordinary cells, i.e. based on the prioritization information (column 9, lines 57-64)." Yet, when Applicant disputes that, the Examiner cites "(column 9-10, lines 64-4)," which the Examiner cited with respect to "obtaining prioritization information." Applicant submits the mere "concept" of "prioritization" does not disclose the subject matter recited in claims 2, 18, and 26. Also, as an example, Applicant sees no teaching in the cited portion as to "when OAM cells are buffered as ordinary cells" allegedly leading to the Examiner's apparent conclusion "i.e., based on the prioritization information."

Regarding claims 3, 11, 19, and 27, Applicant submits "Sorinsuo teaches priorities (column 10, lines 30-31) and classes (column 7, lines 42-50)" is inadequate to allege teaching or suggestion as to, for example, "wherein each of the plurality of virtual connections is...." Applicant submits "scheduling can support priorities" does not teach or suggest "...wherein the prioritization information includes class prioritization information." Thus, Applicant submits the Examiner has not made a *prima facie* showing of obviousness.

Regarding claims 4, 12, 20, and 28, while the Examiner states, "Shimojo teaches a chain of buffer pointers...," Applicant notes the Examiner appears to have alleged "buffers" in Shimojo as allegedly teaching "queues." In that context, Applicant submits Shimojo's purported "chain of buffer pointers" cannot disclose, for example, "wherein each of the plurality of queues is a linked list...." Also, as an example, Applicant notes the cited portion of the cited reference merely states "Each one of the cell groups and the idle buffer pointer chain 251 is provided in the form of a chain of buffer pointers...." Applicant sees no mention of "linked list" to support the Examiner's apparent conclusion of "i.e., linked list."

Regarding claims 5, 13, 21, and 29, Applicant submits claims 5, 13, 21, and 29 do not claim "prioritization" as a "concept." Rather, Applicant submits the cited portions of the cited reference do not appear to disclose, for example, "wherein the prioritization information allocates available bandwidth on the merged virtual connection based on class." Also, as an example, while the Examiner cites "(column 7, lines 42-50)," Applicant sees no mention of "prioritization" in such portion.

Regarding claims 6, 22, and 30, Applicant submits the cited portion of the cited reference appears to refer to a "buffer state list" only in the context of non-prioritized operation. Applicant submits the teachings of

the cited portion of the cited reference that pertain to "priorities" appear not to mention a "buffer state list." Thus, Applicant submits the Examiner's assertions appear not to be supported by the cited portions of the cited reference. Also, as an example, Applicant sees no allegation by the Examiner of any element of the cited portion of the cited reference as purportedly disclosing or suggesting "a prioritization table that stores an accessing sequences for the plurality of queues." Thus, Applicant submits the Examiner has not made a *prima facie* showing of obviousness.

Regarding claims 8, 24 and 32, as an example, Applicant does not see teaching in the cited portion as to "determining that data that constitute a complete packet are buffered."

Regarding claims 9 and 33, even in "column 9, lines 39-51," as cited by the Examiner, Applicant sees no teaching, for example, of "...by combining the data stream...." Also, as an example, Applicant submits the cited portions of the cited references fail to disclose or suggest "generating a data stream...." Thus, Applicant submits the Examiner has not made a *prima facie* showing of obviousness.

Regarding claim 14, Applicant submits mere teaching of, for example, "priority control among classes" in column 24, lines 45 and 46, of the Shimojo reference does not disclose or suggest "wherein the prioritization information causes transitions between classes...." Thus, Applicant submits the purported teachings of the Shimojo reference, even if an attempt were made to combine them with the purported teachings of the Sorinsuo reference, would not yield the subject matter of claim 14. Also, as an example, Applicant submits a mere mention of "priorities" does not teach or disclose "the prioritization information causes...." Thus, Applicant submits the Examiner has not made a *prima facie* showing of obviousness.

Regarding claims 15 and 16, Applicant submits the cited portion of the cited reference that states, "...may be implemented as a stand-alone chip on the output data path..." teaches away from, for example, "wherein the virtual connection merging system is included in the ingress portion of a communication switch." While the Examiner cites "(figure 11, item 1120; column 10, lines 13-15)" and alleges "which is connected to the line interface having input/output ports," Applicant submits such allegation does not teach or suggest "is included in the ingress portion of a communication switch" or "is included in the egress portion of a communication switch."

Regarding claim 34, Applicant submits claim 34 does not recite "a queue/buffer with unlimited size." Therefore, Applicant does not present arguments with respect to such feature. Also, as an example, Applicant submits the cited portions of the cited references fail to disclose or suggest "limiting a number of times the identity of the virtual connection may be queued in the queue." Applicant notes the Examiner states "Shimojo inherently teaches...." While the Examiner asserts a rejection based on inherency, Applicant submits that the teachings of the cited reference fail to establish inherency in accordance with existing law. For example, Applicant submits that the Examiner has failed to establish that the public gained the benefit of the subject

matter recited in claim 34 from the teachings of the cited reference. *Schering Corp. v. Geneva Pharmaceuticals*, 339 F.3d 1373 (Fed. Cir. 2003). As another example, Applicant submits that the Examiner has failed to establish that the subject matter recited in claim 34 is present in the teachings of the cited reference. *Mentor v. Medical Device Alliance*, 244 F.3d 1365 (Fed. Cir. 2001); *Scaltech v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999). Thus, Applicant submits that the subject matter recited in claim 34 cannot be considered to be inherent in the teachings of the cited reference. Accordingly, Applicant submits the Examiner has failed to satisfy the burden of proof required for asserting a rejection based on inherency.

Regarding claim 35, for example, Applicant submits such mere mention of priorities does not disclose or suggest the subject matter recited in claim 35. Thus, Applicant submits the Examiner has not made a *prima facie* showing of obviousness.

Regarding claim 36, while the Examiner additionally cites "flows may include VCCs and different classes (column 20, lines 1-9)," Applicant submits such teaching still does not teach or suggest, for example, "incrementing a pointer within a prioritization information table." Also, as an example, Applicant submits the cited portions of the cited references fail to disclose or suggest "when a first class of the plurality of classes...." Applicant submits the Examiner does not provide evidence as to how the Examiner apparently concludes such teaching purportedly discloses "i.e., class prioritization information." Thus, Applicant submits the Examiner has not made a *prima facie* showing of obviousness.

Regarding claim 37, for example, Applicant submits a mere mention of "priorities" does not teach or suggest "wherein when a particular class has priority, including a predetermined number of packets corresponding to that class in the data stream." Thus, Applicant submits the Examiner has not made a *prima facie* showing of obviousness.

Respectfully submitted,

07/13/2009
Date

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